Holo-interferometric Measurement of the Thermal Deformation Response to Power Dissipation in Multilayer Printed Wiring Boards

by T.D. Dudderar, P.M. Hall and J.A. Gilbert

ABSTRACT—A comprehensive evaluation of the thermally induced warping in two microcircuit modules of differing substructure has been made using holographic interferometry. The measured out-of-plane displacement pattern for the 'symmetric/large-hole' module was found to be very simple, stable, and repeatable, while for the 'asymmetric/small-hole' module it appeared to be highly complex, of changing shape and stable only after several test cycles. Quantitative analysis of these results demonstrate that changes in the internal structure of the multilayer printed wiring board can have a significant impact on the loadings experienced by solder-post connections between the chip carrier and the printed wiring board during normal power cycles. These include changes in the bending pattern sufficient to almost halve the peak Mode B (bending) deformations of the solder posts. At the same time, the associated decreases in local deformation and deformation gradients result in a 33-percent decrease in the peak Mode C (tensile) deformation of these same critical connections.

List of Symbols

a = distance from ceramic-chip-carrier center line to solder post
α = coefficient of thermal expansion
β = half angle between illumination and observation directions
CCI = copper clad invar
$\hat{d}$ = mechanical displacement vector
D = out-of-plane displacement (deformation)
$\Delta\alpha$ = coefficient of thermal-expansion mismatch
ΔT = uniform temperature change (chamber cycling)
h = printed wiring board thickness
H = solder-post height (0.216 mm)
$\hat{\mathbf{i}}_1$ = unit vector along illumination direction
$\hat{\mathbf{i}}_2$ = unit vector along observation direction
$\hat{K}$ = sensitivity vector $(\hat{\mathbf{i}}_1 - \hat{\mathbf{i}}_2)$
λ = wavelength of laser light
n = fringe number
T = temperature

Introduction

Leadless ceramic-chip carriers of the type used in advance-design microcircuit modules have numerous advantages over leaded-device mounting systems.[1-3] These include lower cost, greater ruggedness against handling damage, and simpler, more compact structures with fewer joints. However, the solder posts connecting a leadless ceramic-chip carrier to its multilayer printed wiring board experience significant strains during normally occurring temperature changes, and these can lead to cracks and early failure.[4,5] Assuming the printed wiring board is structurally symmetric, such strains arise primarily because of differences in the thermal-mechanical responses of the leadless ceramic-chip carrier and the printed wiring board, and can be attributed to: (a) the large difference in the thermal-expansion characteristics of these components (most notably during thermal chamber or oven cycling[6]) and (b) the development of large temperature gradients (most notably during power cycling[7]). The incorporation of two symmetrically disposed copper-clad invar (CCI) layers, each of around 140-μm total thickness, into the sublayer structure of the multilayer printed wiring board provides a direct mechanical means of reducing the thermal-expansion-mismatch part of the problem.

As stated in Ref. 7, the transverse or in-plane thermal-expansivity mismatch, $\Delta\alpha$, between a leadless ceramic-chip carrier and a CCI printed wiring board is around 6 ppm/°C. If the ceramic-chip carrier and the printed wiring board were free of each other, their relative fractional expansion would be $6 \times 10^{-6}\ \Delta T$ for a uniform temperature change of ΔT. However, since they are connected the interconnecting solder posts must accommodate any of this differential movement not otherwise accommodated by the in-plane deformation and out-of-plane warping of the ceramic-chip carrier and its printed wiring board. This accommodation may be described in terms of the three modes of deformation shown in Fig. 1.* These modes are identified as: Mode A, associated with the in-plane displacement (or shear), Mode B, associated with the out-of-plane rotation (or bending), and Mode C, associated with the out-of-plane displacement (or tension and compression). In previous studies[6,7] of other module configurations, Mode A deformations have been evaluated from strain-gage measurements made during both chamber and power cycling tests, while holographic interferometry

T.D. Dudderar (SEM Fellow) is Member, Technical Staff, AT&T Bell Laboratories, Murray Hill, NJ 07974. P.M. Hall is Member, AT&T Bell Laboratories, Allentown, PA 18103. J.A. Gilbert (SEM Member) is Professor, University of Wisconsin-Milwaukee, Milwaukee, WI 53201.

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This figure is drawn assuming that the ceramic-chip carrier remains essentially flat while the printed wiring board deforms out-of-plane, which, while not true in general, is reasonable for the mechanical mounting conditions of this study.

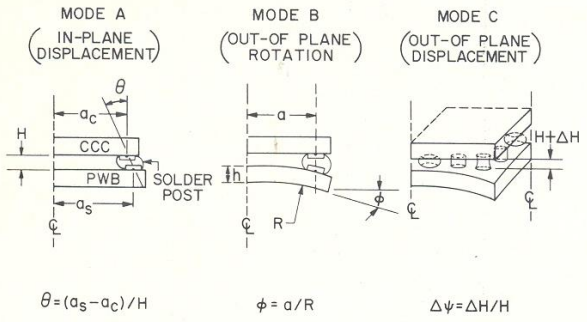


Fig. 1—Solder-post deformation modes for power heating

has been used during power cycling tests to make out-of-plane displacement-field measurements from which Modes B and C could be calculated. It was seen that in a square array of solder posts the corner joints experience the greatest Mode A deformation, being the farthest apart. Bending of the multilayer printed wiring board causes the straight row of posts along any side of a leadless ceramic-chip carrier to experience a varying distribution of Modes B and C as well. Furthermore, in chamber cycling, where the effects of the expansion mismatch dominate, Mode B goes positive with increasing temperature while the printed wiring board bends away from the ceramic-chip carrier at its center. On the other hand—during power cycling where the temperature gradients become significant—as the temperature increases Mode A remains positive, but the printed wiring board bends towards the ceramic-chip carrier at its center as shown in Fig. 1; Mode B goes negative; while Mode C ranges from tension at the corners to compression in the middle.

The present study examines in detail the thermal responses of two different microcircuit module samples subjected to power cycling. The testing process involves the use of holographic interferometry (HI) to determine the out-of-plane* surface-displacement distribution that develops during the resulting heating of the module. The two sample modules, SP1 and SP2, although of the same general configuration, differed in several aspects of varying importance. The multilayer printed wiring board in SP1 had an asymmetric 'stackup', whereas the printed wiring board of SP2 had a symmetric 'stackup'. This means that the distribution of epoxy-glass fabric layers (and copper circuitry) that make up the printed wiring boards of the two sample modules were measurably different in a way that might be expected to influence their structural responses. Furthermore, the critically important clearance holes in the CCI sublayers were of different diameter, with those in SP2 being almost 20-percent larger than those in SP1. A square pattern of these holes is provided in the CCI layers to prevent shorting between these structural elements and the pattern of plated-through-holes that electrically interconnect the various layers of copper circuitry in the printed wiring board beneath the ceramic-chip carrier. Moreover, there were also some slight differences in printed-wiring-board thickness, resin content and the fabric-related anisotropic coefficients of thermal expansion of the two printed wiring boards. Detailed information describing these two samples is given in Tables 1, 2 and 3. Most significantly, the SP1 printed-wiring-board top laminate (meaning the epoxy-glass layers nearest to the printed-wiring-board surface to which the ceramic-chip carrier was mounted) consisted of two intermediate-weight glass-fabric layers, while the bottommost laminate consisted of one very heavyweight glass-fabric layer and one very lightweight glass-fabric layer. SP2 did not exhibit this asymmetry. On the other hand, the larger diameter CCI-layer clearance holes in the SP2 module interact with the limited hole-to-hole spacing of the standard plated-through-hole pattern so as to significantly reduce the substructural stiffening provided to the SP1 printed wiring board by the internal CCI layers in the critical region directly below the ceramic-chip carrier.

The large outermost laminate-layer asymmetry in SP1 would be expected to enhance warping of the printed wiring board (regardless of the presence of ceramic-chip carriers) even under conditions of uniform, gradient-free heating. Such enhanced warping would involve two components, one arising from the asymmetry in bending compliance, and the other arising from the asymmetry in thermal expansivity. Predicting the net thermal response for an unconstrained printed wiring board during uniform heating would be difficult at best. Under the conditions of highly localized temperature gradients that occur during power dissipation, together with the complex thermo-mechanical interactions between the surface-mounted leadless-ceramic-chip carriers and the printed wiring board, and the variations in local stiffness associated with differences in the clearance holes, the development of a rational understanding of the thermal response can be achieved only through a comprehensive full-field experimental evaluation. The present study was conducted to exploit the capacity of HI for making such an evaluation. The analysis of the resulting data is focused on determining the rotations and out-of-plane deformations imposed on the interconnecting solder posts by the thermally induced warping of the complex ceramic-chip-carrier/printed-wiring-board structure. Relevant comparisons are drawn between the markedly different responses of the two samples.

The Fiber-Optic Holographic Interferometer

A schematic diagram of the holographic interferometer used in this study to determine the out-of-plane thermal-displacement fields is shown in Fig. 2. Single-mode optical fiber was used in both the object and reference beams for operational flexibility, as well as for long- and short-term stability.[8,9] In this system the complicated array of steering mirrors, prisms and spatial filters usually found in traditional holographic systems has been replaced by two single-mode optical fibers of suitably dissimilar length as required to provide the necessary optical-path-length matching. No spatial filtering was required as the single-mode fibers themselves accomplish that function, as well as relaxing many of the usual stability requirements. So long as the launch optics are firmly coupled to the laser, only the fiber outputs, the test specimen and the hologram itself need be rigidly interconnected and vibration isolated. Furthermore, the free-space (air) propagation path lengths are significantly reduced, so that the deleterious integrated effects of thermal gradients in the

It was considered that the out-of-plane warping would be of greatest interest for those particular samples whose CCI printed wiring boards are designed to suppress most of the in-plane (Mode A) deformation.

air are greatly reduced. In all other ways this interferometer was a standard off-axis holographic system which was operated, except for a few real-time observations, in the double-exposure mode. In this mode the sample to be tested was first illuminated in its initial state (at room temperature and unpowered) with coherent light transmitted from the laser via a single-mode fiber. A hologram was then recorded by exposing a high-resolution photographic film plate positioned at the junction of the reflected light and the reference beam, also transmitted via a single-mode optical fiber. Upon completing this first exposure, power was applied to a resistance circuit on the ceramic-chip carrier and the module was allowed to come to thermal equilibrium as monitored by a thermocouple on the ceramic-chip carrier. At around 20 minutes (although complete thermal stability may require twice that time, and mechanical stability may require even longer) the sample was illuminated again and a second holographic recording was made on the same film plate. Usually the sample was then unpowered and allowed to cool off prior to the next cycle. Finally, after sufficient cycles to various power and/or temperature levels were carried out and recorded on successive plates as desired, the holograms were processed and reconstructed to produce a history of doubly exposed holographic interferograms.

Each resulting holographic-interference-fringe field may be related to the thermal deformations of the surface which occurred during heating by the simple vector expression

$$n\lambda = \hat{k} \cdot \hat{d} \tag{1}$$

where n is the fringe number, λ is the wavelength of coherent light used to record and reconstruct the hologram, $\hat{k}$ is the sensitivity vector $(\hat{1}_2 - \hat{1}_1)$ where $\hat{1}_1$ and $\hat{1}_2$ are unit vectors in the illumination and observation directions respectively, and $\hat{d}$ is mechanical displacement vector at the point of observation on the surface of the sample. In the present tests the nearly plane back surface of the module (printed wiring board and leadless-ceramic-chip carrier) is intentionally oriented normal to the bisector of the angle, 2β, between $\hat{1}_1$ and $\hat{1}_2$. Therefore, since the sensitivity vector, $\hat{k}$, also points along this bisector, the interferometer senses only the out-of-plane displacement component, D. Equation (1) then becomes

$$n\lambda = 2D\cos\beta \tag{2}$$

In the present study the surface normal (at the bisector angle β) is only 3.2 deg off the observation direction and λ is 0.633 μm so that each fringe represents an out-of-plane displacement change of only 0.316 μm.

Test Samples

Sample modules SP1 and SP2 each consisted of a 1.5-mm × 55-mm × 95-mm multilayer printed wiring board (as described by Tables 1, 2 and 3) with a single 16.5-mm × 16.5-mm leadless-ceramic-chip carrier mounted asymmetrically as shown in Fig. 3(a). Figure 3(b) shows the nominal stack-up dimensions in cross section. The leadless-ceramic-chip-carrier standoff height, H, was 0.216 mm. For these tests each sample was provided with a thin-film resistor mounted within its ceramic-chip carrier in place of the microcircuit silicon chip, and each was instrumented with a thermocouple to monitor the temperature rise when the resistor was powered up to simulate operation of the module. The power and thermocouple leads were fed out through thin grooves machined in the walls of each ceramic-chip carrier. A Kovar lid was soft soldered to the top of each ceramic-chip carrier. This provided a firm attachment point. Each sample module was mounted by rigidly bonding its ceramic-chip-carrier lid to a separate 7-mm thick-glass mounting plate. The

TABLE 1—SAMPLE DESCRIPTION

Sample	SP1	SP2
CCI-Clearance Hole Diameter (mm)	1.092	1.372
Thickness of Printed Wiring Board (mm)	1.651	1.549
Resin Content (Weight percent)	61.4	58.7
Avg. X TCE* (ppm/ °C)	11.3	11.5
Avg. Y TCE (ppm/ °C)	11.7	11.2
Avg. XY TCE (ppm/ °C)	11.5	11.4

*TCE = Thermal Coefficient of Expansion

TABLE 2—PRINTED-WIRING-BOARD STACKUPS [see Fig. 3(b)]

	SP1		SP2	
Epoxy-Glass Stackup	No. of Fabric Layers	Glass-Fabric Styles*	No. of Fabric Layers	Glass-Fabric Styles
Laminate† (C-Stage)	2	2116	1	7628
			1	104
Prepreg (B-Stage)	1	104	1	104
	3	108	3	108
	1	104	1	104
Laminate (CCI C-Stage)	2	108	2	108
Prepreg (B-Stage)	1	104	1	104
	3	108	3	108
	1	104	1	104
Laminate (C-Stage)	1	104	1	104
	1	7628	1	7628

*The fiberglass fabric styles are described in Table 3.
†This is the epoxy-glass laminate nearest the ceramic-chip carrier surface of the printed wiring board [next to the top riston layer in Fig. 3(b)].

TABLE 3—GLASS-FABRIC DESCRIPTION

Glass-Fabric Style Number	Construction Threads/Inch		Average Fiber Diameter		Average Fabric Thickness	
	X-Direction	Y-Direction	(mils)	(μm)	(mils)	(μm)
104	60	52	0.23	5.8	1.2	30.5
108	60	47	0.23	5.8	2.0	50.8
2116	60	58	0.23	5.8	4.0	101.6
7628	44	32	0.38	9.7	6.8	172.7

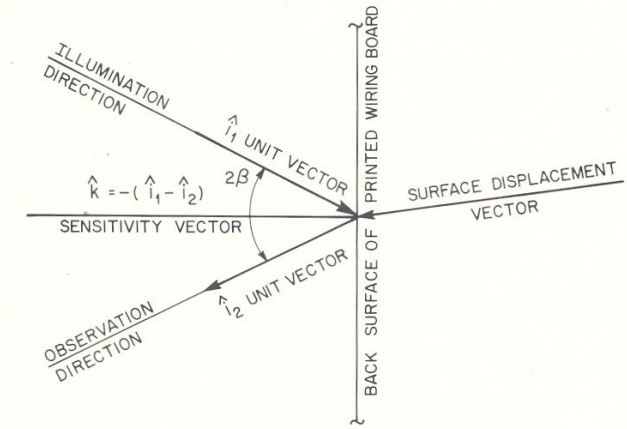
reverse or back surface of the sample printed wiring board was spray painted white to improve reflectivity at the operating wavelength. This assembly could be mounted in the interferometer as needed for HI testing. A series of doubly exposed holograms of the back of the printed wiring board of each sample were recorded as described above. In this configuration the ceramic-chip carrier was supported by the vertical glass mounting plate while the printed wiring board was supported by the solder posts connecting it to the ceramic-chip carrier.

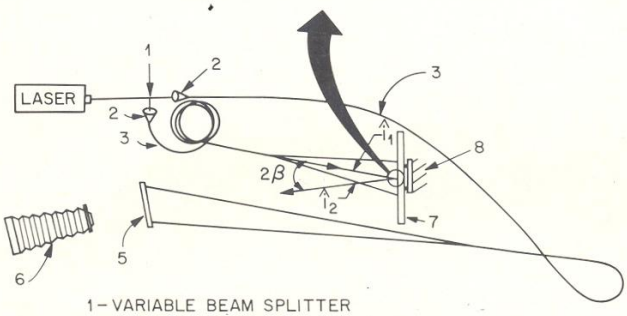
In actual service such a module would be supported by a much larger 'mother' board (designated CIC) and the ceramic-chip carrier would be supported solely by the solder posts. This actual mounting is generally accomplished by means of parallel rows of pin interconnections to the mother board (called CIC) running along the long sides of the module's printed wiring board, and represents a somewhat more constrained mounting condition than that of the 'free' mounting system used in the present study. As described elsewhere,[7] the authors have also carried out holo-interferometric thermal-deformation studies with modules that were clamped rigidly along their long sides, a boundary condition of significantly greater constraint than the actual 'on CIC' mounting condition. Because both the CIC board and the pin interconnections are somewhat compliant (to a degree dependent on the specific design and packaging), the boundary conditions for an actual module mounted on its CIC mother board lie between the 'free' and 'edge-clamped' boundary conditions. A holo-interferometric thermal-deformation study of the effect of the three mounting systems has been carried out using modules of earlier design with a different printed wiring board.* These studies, whose quantitative nature are specific to that design, happened to yield Mode B and Mode C deformations for the 'on CIC' boundary conditions that were 60 percent to 70 percent as large as those obtained using the 'free' boundary conditions. Furthermore, it has been found through many tests that the 'free' mounting system is the most sensitive to structural variations, gives most reliable, repeatable results and is generally the most practical to apply. Since it was also the most conservative, providing an 'upper bound' on the magnitude of the response, this mounting system was adopted for all tests in the present study.

Experiments

Sample module SP1, described as the 'asymmetric/small-hole' sample, was tested first. Three successive

These boards had no CCI layer to restrain their in-plane expansion.





1-VARIABLE BEAM SPLITTER
2-FIBER LAUNCH OPTICS
3-SINGLE MODE OPTICAL FIBER
4-CERAMIC CHIP CARRIER
5-HOLOGRAM PLATE
6-CAMERA SYSTEM
7-PRINTED WIRING BOARD

Fig. 2—Schematic of the fiber-optic holographic interferometer used to record and reconstruct the holographic interferograms

cycles to full power (0.75 W) were recorded on three successive doubly exposed holograms, reconstructions of which appear in Fig. 4. Three cycles to full power were made on the 'symmetric/large-hole' sample SP2, the first and the last of which were recorded holographically and reconstructed as shown in Fig. 5. Finally, both samples were tested to half power. Figure 6 shows reconstructions of the resulting holographic interferograms.

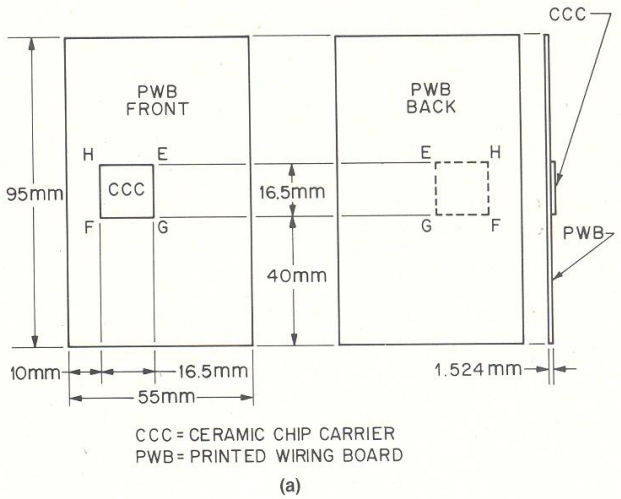
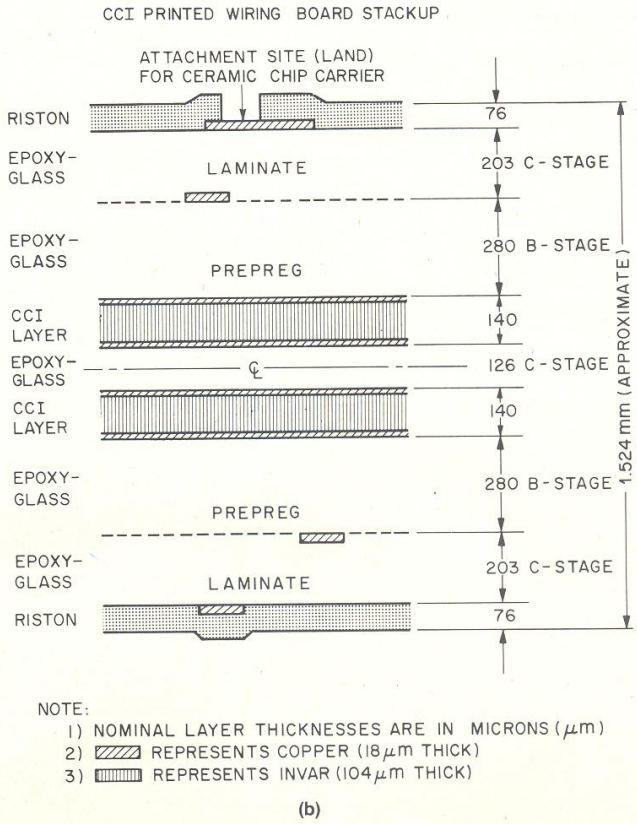


Fig. 3—The microcircuit sample module: (a) diagram showing location of ceramic-chip carrier, and (b) printed-wiring-board layer structure showing locations and CCI inserts



Discussion

Printed-Wiring-Board Out-of-Plane Deformation Field

In all of the holographic-fringe data pictured in Figs. 4, 5 and 6, the location of the ceramic-chip carrier on the printed-wiring-board-surface way from the camera is clearly indicated by a local extremum just to the right of the center of the printed wiring board. The direction (in- or out-of-plane) of this extremum cannot be determined from these doubly exposed holographic interferograms alone. However, by visually observing the direction of fringe movement when manual pressure was applied to the surface during a real-time test, it was determined that during heating the printed wiring board does in fact bend towards the ceramic-chip carrier in the center, as shown in Fig. 1(b). Since this represents an out-of-plane deforma-

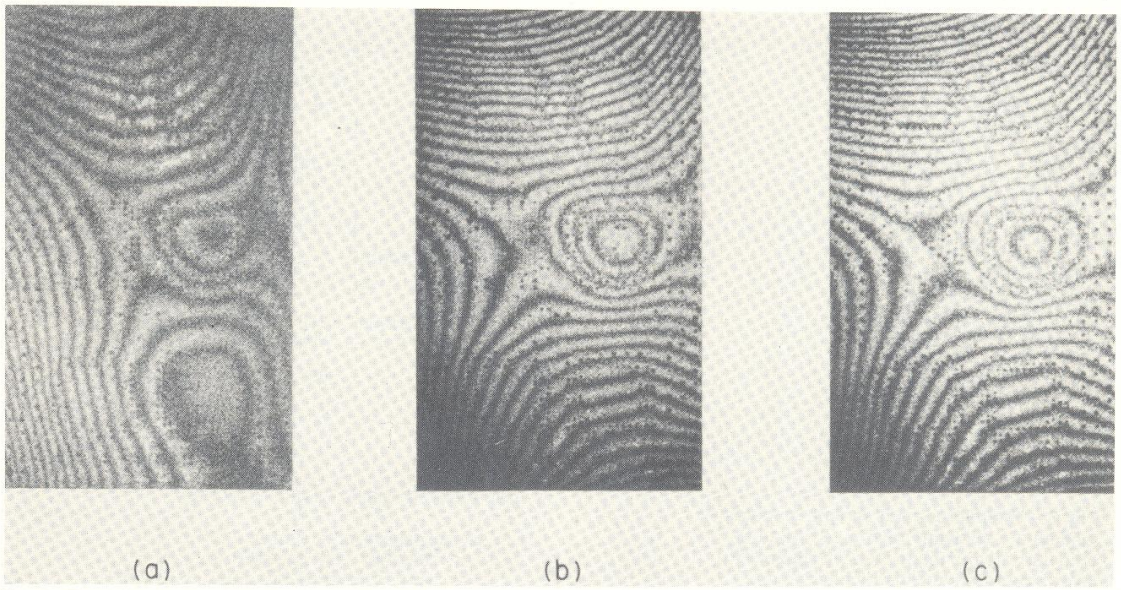


Fig. 4—Reconstruction of the holographic interferograms for SP1 powered to 0.75 W for 20 minutes for the (a) first cycle, the (b) second cycle and the (c) third cycle

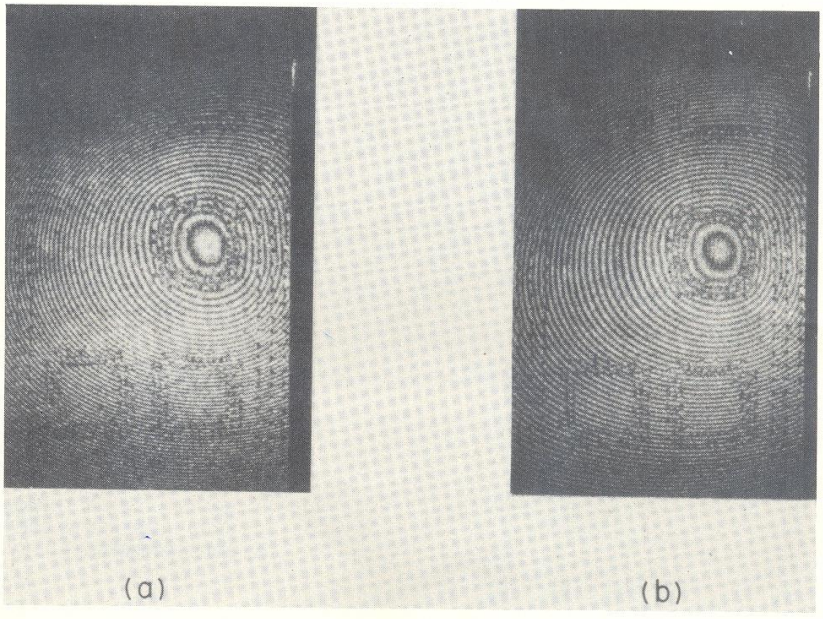


Fig. 5—Reconstruction of the holographic interferograms for SP2 powered to 0.75 W for 20 minutes for: (a) first cycle, and the (b) third cycle

tion as seen from the ceramic-chip carrier side, it will be referred to as a 'hill' beneath the ceramic-chip carrier.

It is immediately apparent from Fig. 4 that the asymmetric/small-hole sample-module SP1 experiences significant changes in both the out-of-plane deformation distribution and magnitude with each successive cycle, indicating that some 'shakedown' is involved in reaching a stable thermal response. It should be noted that the shapes of the stabilized holographic fringe patterns on the first cycle to full power [Fig. 4(a)] and the later cycle to half power [Fig. 6(a)] are quite similar in that each exhibits an 'extremum' (a valley as seen from the front, a hill from the back) in the lower half of the printed wiring board. This feature is largely absent from the interferograms taken on subsequent cycles to full power and shown in Figs. 4(b) and 4(c). Real-time observation on a subsequent cycle to full power revealed the initial presence of this 'valley' region which moved off the bottom of the printed wiring board as the temperature increased and stabilized.

On the other hand, the interferograms of SP2 are regular and clearly remain very nearly the same from cycle to cycle as shown in both Fig. 5 (at full power) and Fig. 6(b) (at half power), which differ only in fringe density. The real-time observations showed much the same morphology and stability, again differing only in fringe density from the patterns shown in Figs. 5 and 6(b). An even greater contrast in behavior is to be seen in the magnitude of the response of the two sample modules, with SP2 showing far greater deformation than SP1. As a global comparison, consider the peak or maximum deformation as it appears in the upper left-hand corner of the printed wiring board in the maximum power interferograms for each sample module as shown in Figs. 4 and 5, which shows a more than threefold increase in thermal-deformation response associated with the differences between SP1 (as stabilized) and SP2. A tabulation of these peak displacements for all the tests run with these samples is given in Table 4, along with the imposed power levels and associated ceramic-chip-carrier temperature increases as measured 20 minutes after the power was applied.

More comprehensible pictorial representations of the printed-wiring-board warping and overall deformation can be seen in Fig. 7. In Fig. 7 isometric computer reconstructions of the resulting out-of-plane deformation fields are shown for SP1 on the first [Fig. 7(a)] and third [Fig. 7(b)] full-power cycles [derived from the holo-

TABLE 4—MAXIMUM OUT-OF-PLANE DISPLACEMENT* AFTER TWENTY MINUTES AT 0.75 W

Event (Cycle)	Power (W)	SP1		SP2	
		ΔT (°C)	Δ (μm)	ΔT (°C)	Δ (μm)
1st	0.750	19.3	4.1	19.3	24.3
2nd	0.750	19.5	7.3	19.7	NR†
3rd	0.750	19.7	7.6	19.6	23.4
1st	0.375	10.4	3.2	9.3	7.3
2nd	0.375	NR	NR	9.7	7.3
1st	0.690	NR	NR	18.2	16.8
2nd	0.690	NR	NR	18.4	16.1

**As measured at the upper left-hand corner of the printed wiring board when viewed from the back (Figs. 5 and 6). This was the region of maximum thermal response for both sample modules*
†NR—never run or not recorded holographically

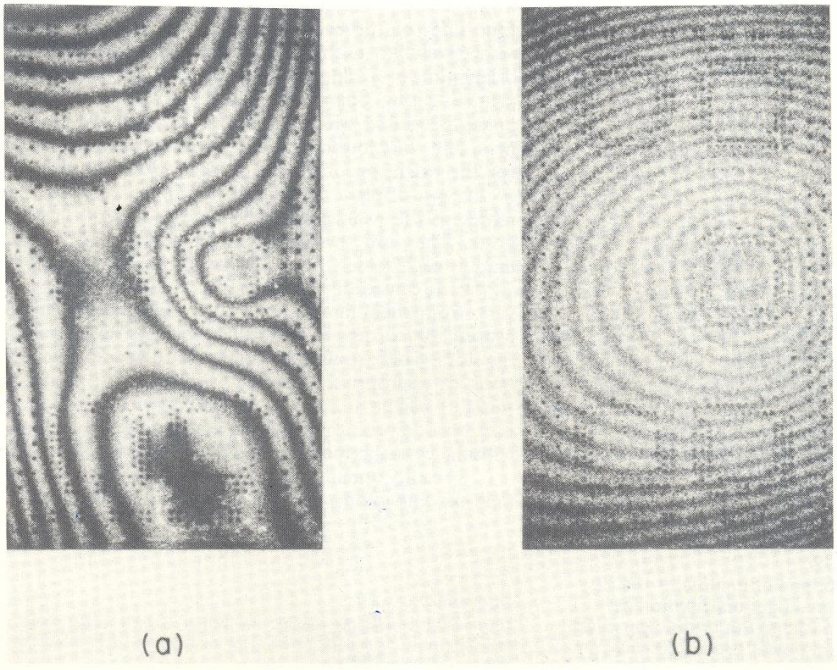


Fig. 6—Reconstruction of the holographic interferograms for the first-power cycle to 0.375 W for 20 minutes for: (a) SP1, and (b) SP2

graphic interferograms shown in Figs. 4(a) and 4(c)]. Here the deformation is shown as positive, representing the displacement of the front (rather than back) surface of the printed wiring board, and with a highly exaggerated* vertical scale. It appears that the distinct local curvature which results from the strong thermal gradients below the ceramic-chip carrier are at least partially countered by a reverse curvature or warping. Figure 7(c) shows the same type of computer-generated isometric reconstruction of the out-of-plane deformation of SP2 derived from the interferogram at full power [Fig. 6(a)], but at *one-fourth* the vertical scale. This far more regular geometry extends the hill shape over the entire printed wiring board, with no out-of-plane bending asymmetry to counter the curvature.

**Scales are shown in the figures, with the vertical scales around 1000 times the horizontal scales.*

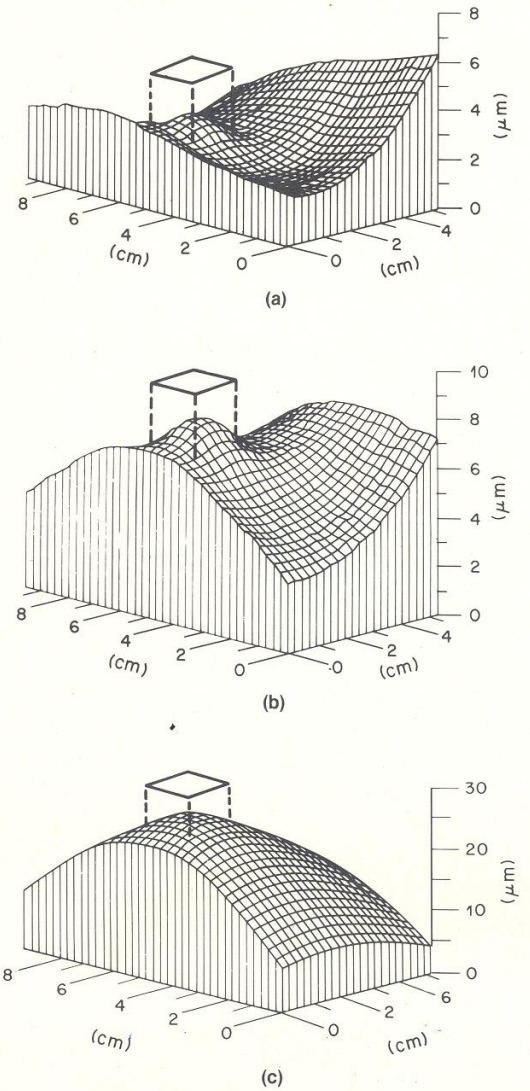


Fig. 7—Computer-generated isometric plots of the HI measured out-of-plane displacement distribution as viewed at an angle of 15 deg for: (a) the first-power cycle to 0.75 W on SP1, (b) the third-power cycle to 0.75 W on SP1, and (c) the first-power cycle to 0.75 W on SP2

Solder-Post Deformations

While the peak printed-wiring-board corner deflections given in Table 4 and the computer graphics shown in Fig. 7 clearly illustrate substantial differences in thermal response associated with differences between SP1 and SP2, they provide only extreme comparisons. In fact, it would be expected that the overall thermal-response characteristics of a microcircuit module in actual service would be somewhat different, especially considering the effects of the actual mounting and the presence of four or five more ceramic-chip carriers on the printed wiring board. These additional ceramic-chip carriers represent regions of increased stiffness which also act as supplemental heat sources (albeit at substantially lower power levels†) and influence the overall thermal-deformation field away from the central ceramic-chip carrier (which dissipates most of the power). Of much greater significance, then, is the distribution of deformation and deformation gradients local to this primary ceramic-chip carrier which contribute to the Mode B and Mode C deformations of the solder posts. Figures 8(a) and 8(b) show plots of the deformation distributions along the primary longitudinal (vertical) and transverse (horizontal) axes through the ceramic-chip carrier from which slopes defining the Mode B bending of the center-line solder posts for each sample were calculated as defined in Fig. 1. Similar evaluations of the slopes along the ceramic-chip-carrier diagonal directions provided Mode B determinations for the solder posts nearest the corners of the ceramic-chip carrier where the out-of-plane deformations were greatest. These results are tabulated in Table 5, where the ceramic-chip-carrier corner positions are identified as E, H, F, and G and the side positions are identified as E-H, H-F, F-G, and G-E as shown in Fig. 3(a). Figures 9(a) and 9(b) show profiles of the out-of-plane deformation distributions plotted around the four sides of the ceramic-chip carrier for SP1 and SP2 respectively. In each case a 'tilt' plane representing the orientation of a rigid ceramic-chip carrier relative‡ to the printed wiring board was calculated by identifying the plane associated with the best fit through the four corners, and then lowering it until it gave a net sum of zero for the extension of all the solder posts. The deviations of the out-of-plane deformation profile from this plane represent the extensions (or compressions) of the solder posts. They are shown in the figures as heavy vertical lines at each solder-post location around the ceramic-chip carrier. It can readily be observed that these deformations vary from their maximum tensile values at solder posts nearest the corners to generally compressive values along the sides. These results are converted to Mode C deformations of appropriate sign by dividing by the solder-post standoff height, 0.216 mm. These corner and side-solder-post Mode C deformations are included in Table 5, along with the corresponding Mode B deformations.

It is readily apparent from these results that the magnitude of both modes of solder-post deformation are sub-

†Approximately 0.2 W

‡In these tests, with the ceramic-chip carrier bonded to the heavy glass mounting plate, it may be taken to be substantially rigid in comparison with the printed wiring board.

stantially different for these two samples. On the other hand, even picking the worst cases, the differences were not nearly as great as those observed with the overall results developed earlier and presented in Table 4. It may be concluded then, that while the increases in deformation associated with the structural changes are significant, they are properly defined by the local conditions at the solder posts (Table 5) rather than the global maxima (Table 4) on the printed wiring boards.

Summary and Conclusions

Holo-interferometry provides a powerful tool for the quantitative, detailed evaluation of the mechanical characteristics of microcircuit modules. In the present study it is apparent that the thermal response of module sample SP1 is quite different from that of sample SP2, with SP1 being by far less regular in almost all respects. While other, less significant, structural differences exist between these two test samples, the most likely contributors to this result are the fundamental differences between printed-wiring-board stackup asymmetry and CCI-layer-clearance hole

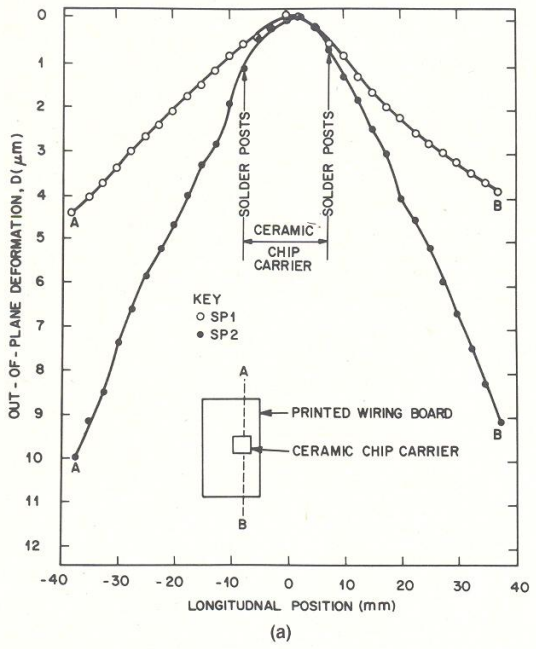


Fig. 8—Plots of the thermal-deformation distribution after 20 minutes at 0.75 W as measured along a: (a) longitudinal center line A-B, and a (b) transverse center line C-D

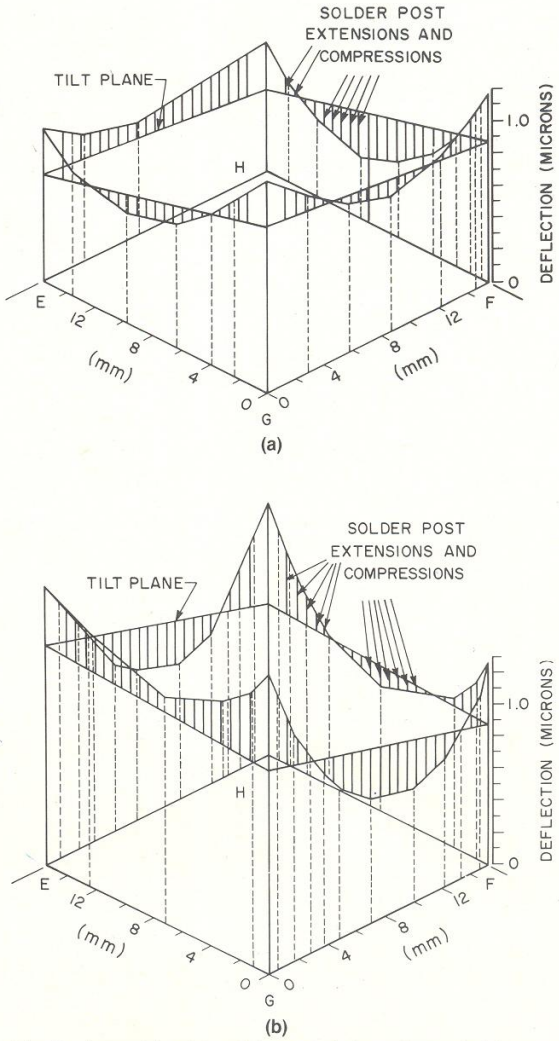


Fig. 9—Isometric plots of the out-of-plane thermal deformation of the printed wiring board at the solder posts connecting the ceramic-chip carrier after 20 minutes at 0.75 W for: (a) SP1, and (b) SP2

TABLE 5—MAXIMUM MODE B AND MODE C SOLDER-POST DEFORMATIONS AFTER 20 MINUTES AT 0.75 W

Sample Module and Test	Deformation Mode	Solder-Post Location [See Fig. 3(a)]							
		E (Corner)	E-H (Side)	H (Corner)	H-F (Side)	F (Corner)	F-G (Side)	G (Corner)	G-E (Side)
SPI	B (milliradians)	−0.122	−0.112	−0.099	−0.050	−0.185	−0.136	−0.110	−0.110
3rd Cycle	C (%)	+0.100	+0.016	+0.120	−0.110	+0.083	+0.046	+0.090	−0.056
SP2	B (milliradians)	−0.270	−0.256	−0.212	−0.263	−0.255	−0.216	−0.256	−0.240
1st Cycle	C (%)	+0.134	−0.125	+0.185	−0.060	+0.083	−0.139	+0.194	+0.046

diameter. The following observations may be made as to the effects of these substructural differences on the thermal response of the microcircuit module and the associated deformations of the critical solder-post connections between their surface-mounted ceramic-chip carrier and the printed wiring board.

(1) It appears that there is a significant effect on the stability of the thermal response. (a) For asymmetric/small-hole sample module SP1 the thermal-deformation distribution changed significantly from the first to the second cycle to full power (0.75 W). For symmetric/large-hole sample module SP2 this distribution remained essentially unchanged for the same circumstances. (b) For SP1 the maximum thermal-deformation magnitude increased by almost 85 percent from the first to the second cycle to full power, while for SP2 it was essentially unchanged. (c) For SP1 the thermal-deformation pattern (magnitude and distribution) approached stability in subsequent cycles to full power, while for SP2 it was essentially stable from the start. (d) For SP1 both the magnitude and the distribution of the thermal deformation changed during heating. (The holo-interferometric fringe field became denser and changed shape.) For SP2 only the thermal-deformation magnitude increased with heating, while the distribution remained essentially the same. (The holo-interferometric fringe field became denser but retained its shape.)

(2) The maximum out-of-plane warping of the printed wiring board is significantly reduced by the effects of laminate asymmetry and/or the smaller clearance hole diameter. (a) The maximum out-of-plane thermal deformation of the printed wiring board was only 8 μm for the asymmetric/small-hole sample-module SP1 vs. 25 μm for the symmetric/large-hole sample-module SP2—a very large difference. (b) For SP1 the thermal-deformation pattern is complex with a saddle region and evident anti-plane bending which changes with successive cycles and/or power levels. For SP2 it is much simpler—almost rotationally symmetric about the ceramic-chip carrier mounting region—and quite repeatable.

(3) The local conditions defining the critical solder-post deformations are also different, although less severely than the overall out-of-plane warping would indicate. (a) The averaged Mode B (out-of-plane bending) deformation of the connecting solder posts nearest the corners of the ceramic-chip carrier where the maximum occurs reached 0.13 milliradians for asymmetric/small-hole sample-module SP1 vs. 0.25 milliradians for symmetric/large-hole sample-module SP2 as measured at full power after 20 minutes, a difference of almost 95 percent. (b) The averaged maximum Mode C (out-of-plane tensile) deformation of the connecting solder posts at the corners of the ceramic-chip carrier where the tensile maximum occurs reached 0.10 percent for SP1 and 0.15 percent for SP2 as measured at full power after 20 minutes, a difference of 50 percent. (c) The averaged maximum negative Mode C (out-of-plane compressive) deformation of the connecting solder posts along the sides of the ceramic-chip carrier reached −0.05 percent for SP1 vs. −0.08 percent for SP2 at full power after 20 minutes, a significant difference.

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