Whole Field Deformation in Printed Wiring Boards†

T. D. Dudderar
AT&T Bell Laboratories
600 Mountain Avenue
Murray Hill, New Jersey 07974

J. A. Gilbert
Associate Professor of Engineering Mechanics
University of Wisconsin-Milwaukee
Milwaukee, Wisconsin 53201

P. M. Hall
AT&T Bell Laboratories
555 Union Boulevard
Allentown, Pennsylvania 18103

D. R. Matthys
Associate Professor of Physics
Marquette University
Milwaukee, Wisconsin 53233

ABSTRACT

Holographic interferometry is used to study thermally induced deformations in multilayer printed wiring boards with surface mounted ceramic chip carriers during power on/power off cycles. Results demonstrate that both the number of chip carriers and the internal structure of the wiring board can strongly influence the response.

INTRODUCTION

Micro-electronic modules with leadless components surface mounted to printed wiring boards may experience significant thermally induced warping and deformation during manufacture and subsequent service. Such behavior may impose severe loadings on the solder interconnections between the components and the mounting board which can result in rapid fatigue and premature failure. These deformations usually arise because of differences in the thermal-mechanical responses of the surface mounted components and the printed wiring board. Generally the printed wiring board exhibits a greater coefficient of thermal expansion, α, than any given surface mounted component. Consequently, increases in ambient temperature generate geometrical mismatches which put surface mounted components into tension and cause the printed wiring board itself to bend out-of-plane and locally away from the components.* On the other hand, active components which dissipate power may generate large local thermal gradients in the printed wiring board itself which can also cause it to bend out-of-plane, but in the opposite direction. Actual service conditions usually involve both of these bending phenomena in varying proportions, so they may, to some extent, locally offset one another. Unfortunately, the net mechanical response depends on many material and structural factors, including the printed wiring board's own laminate layup and mounting, as well as the design, number and placement of the surface mounted components. Such complexity makes reliable mathematical or numerical

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* This assumes that the module is fully relaxed and stress free at the start of the power cycle. Naturally, the existence of residual stresses remaining from manufacture or previous cycles of thermal loading can be expected to complicate this scenario.

thermal stress analysis difficult if not impossible, and a valid understanding of the actual thermal mechanical behavior of such a system inevitably requires careful experimental evaluation of prototype designs.

If the thermal expansion mismatch, $\Delta\alpha$, is large, as with leadless ceramic chip carriers ($\alpha \simeq 5.5$ ppm/°C) soldered directly to a fiber glass-epoxy printed wiring board ($\alpha \simeq 20$ ppm/°C), good design practice may involve the use of a board whose laminate structure incorporates sublayers of copper clad invar (CCI) with an $\alpha \simeq 5$ ppm/°C. This provides a direct mechanical constraint on its in-plane thermal expansivity and significantly reduces the geometrical mismatch aspect of the warping problem. However, the thermal gradient aspect remains and may in fact be somewhat aggravated by too close a match between the coefficients of thermal expansion, especially for high power surface mounted components that produce large local thermal gradients in the printed wiring board. In order to study these effects the present program to compare the thermal mechanical responses of various prototype designs was carried out using holo-interferometry to make whole-field deformation measurements. Various reports of earlier successful applications of this technique to studies of the effects of heat generated in micro-electronics have been published elsewhere.[1,2,3,4]

THE EXPERIMENTS

Four prototype modules were prepared using two types of multilayer printed wiring boards: two without CCI sublayers ($\Delta\alpha \simeq 15$ ppm/°C) and two that were otherwise identical but with CCI sublayers ($\Delta\alpha \simeq 6$ ppm/°C). For each type of board the two sample modules also differed, with one having five symmetrically arrayed leadless ceramic chip carriers as shown in Figure 1, and the other having only the one central ceramic chip carrier. In every case, only the central chip carrier was powered, so that both powered and unpowered surface mounted components were involved in the test program.

In every case the module being tested was mounted vertically by firmly clamping along the two long sides of the printed wiring board (or "edge clamping") as described in an earlier report.[2] In addition, the fiber optic holo-interferometer used in the present study was also the same as the one described earlier,[2,3,4] with single mode optical fiber components used in the object illumination and reference beams for convenience, stability and flexibility. Double exposure holo-interferograms were generated by holographically recording the test module at successive states of power off and power on or power on and power off. Each test module experienced around ten such cycles, and after every cycle the module was allowed 20 minutes to stabilize

before making an exposure. Figure 2 shows reconstructed holo-interferogram images of the front and rear printed wiring board surfaces typical of the two modules without CCI sublayers, while Figure 3 shows similar images of the two modules with CCI sublayers. In every case shown the module was cycled between 0 and 0.75 watts (full power). Each of these images includes a superimposed holo-interferometric fringe pattern which represents a contour mapping of the out-of-plane change of shape or warping of the printed wiring board with a 0.32μ displacement between contour fringes. Figures 4 and 5 show isometric plots of these deformations for the same samples.

DISCUSSION AND RESULTS

It is immediately apparent that, even in these power dissipation tests where thermal gradient effects predominate, the presence of CCI sublayers in the printed wiring boards helps reduce overall warping, especially in the prototype module configuration with the single ceramic chip carrier. Moreover, in both configurations the local "hilling" under the central powered ceramic chip carrier is somewhat suppressed. It is also evident that the presence of additional (unpowered) leadless ceramic chip carriers has a pronounced influence on the global deformation pattern, contributing to a far more complex out-of-plane warping pattern. Careful examination of the holo-interferograms indicates that these added ceramic chip carriers are flexible enough to bend with the board, rather than acting as rigid members whose stiffnesses must be accommodated largely by deformations of the solder interconnections between the ceramic chip carriers and the thermally warped printed wiring board. On the other hand, though passive and relatively flexible out-of-plane, these ceramic chip carriers impose enough of a constraint on the board to alter its mode of buckling and, consequently, still wind up in having a strong influence on the overall deformation pattern.

Finally, in some cases the response varied markedly from test cycle to test cycle. For example, the apparent shape change anomaly exhibited by the printed wiring board with a single ceramic chip carrier and no CCI sublayers (Figure 2 top and Figure 4 right hand side) is actually a manifestation of this cycle-to-cycle change in response, rather than a consequence of some remarkably incompatible deformations of the board's opposing surfaces.

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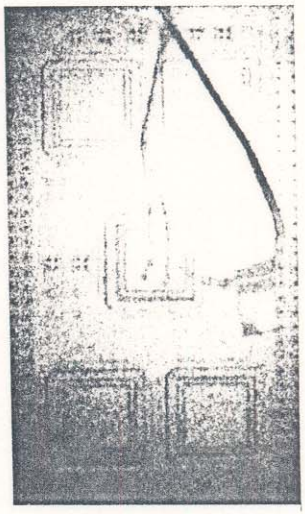

Figure 1. Reconstructed hologram image of a typical prototype module with five leadless ceramic chip carriers in an "edge clamped" mounting.

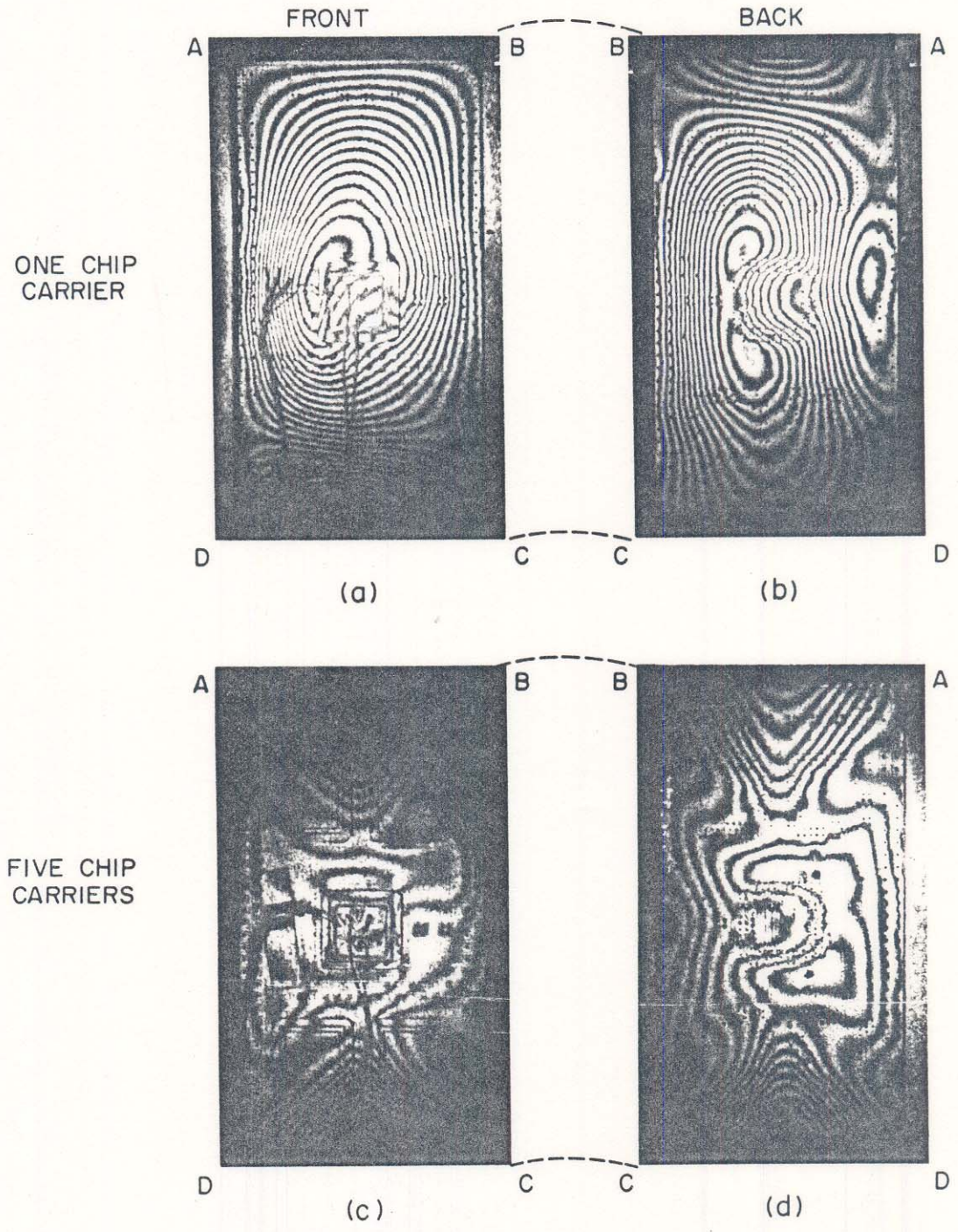

Figure 2. Reconstructed front and back surface holo-interferograms for two prototype modules without CCI sublayers in their printed wiring boards. Both modules were cycled to full power. The resulting temperature rises on the powered ceramic chip carrier for the module with the five chip carriers were 24.7 ± 0.1°C in the front surface test and 25.0 ± 0.1°C in the back surface test. The temperature rises for the module with the single chip carrier were the same, 25.3 ± 0.1°C in both tests.

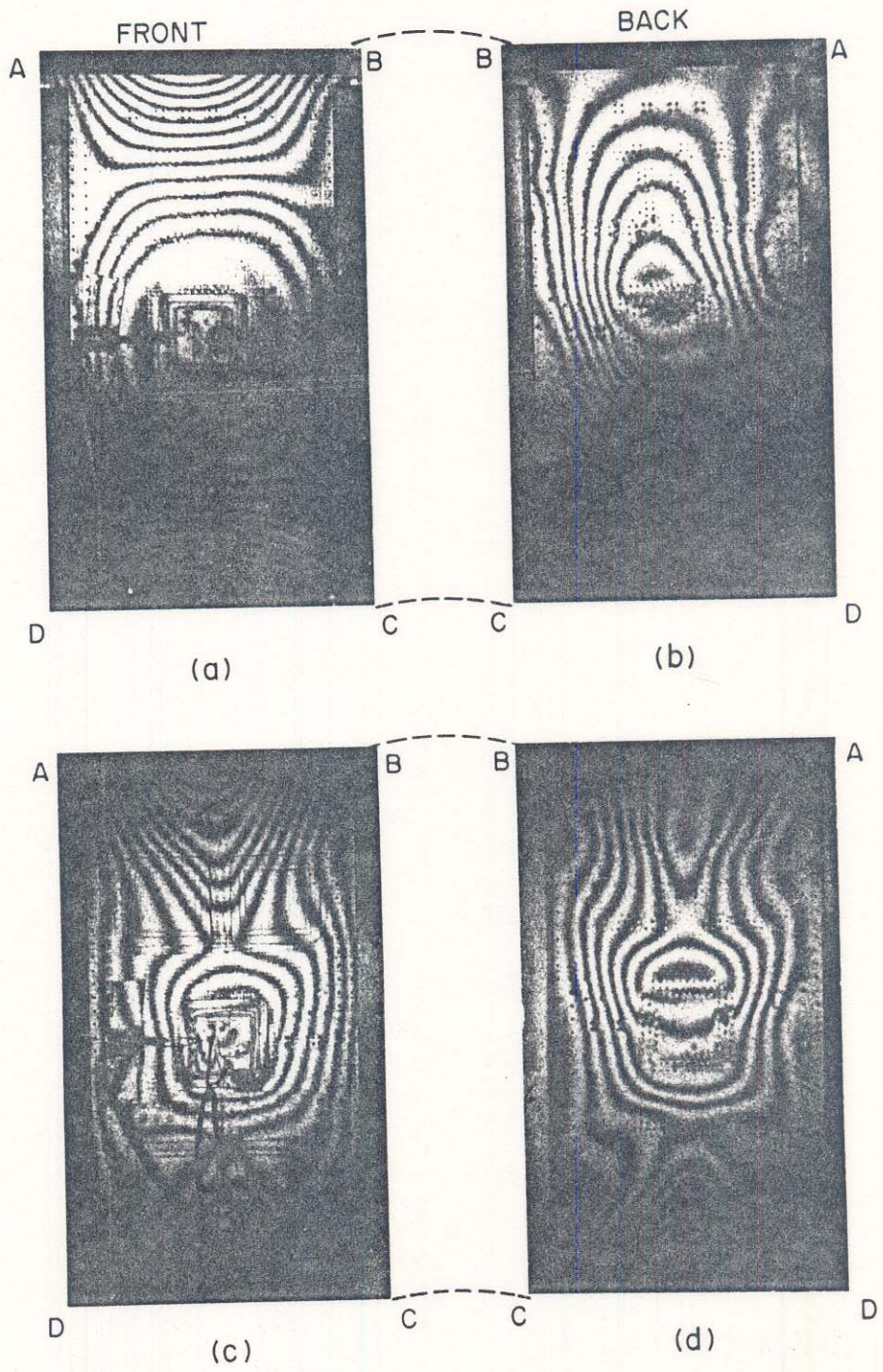

Figure 3. Reconstructed front and back surface holo-interferograms for two prototype modules with CCI sublayers in their printed wiring boards. Both modules were cycled to full power. The resulting temperature rises on the powered ceramic chip carrier for the module with the five chip carriers was 22.0 ± 0.1°C in the front surface test and 22.1 ± 0.1°C in the back surface test. The temperature rises for the module with the single chip carrier were the same, 21.2 ± 0.1°C in both tests.

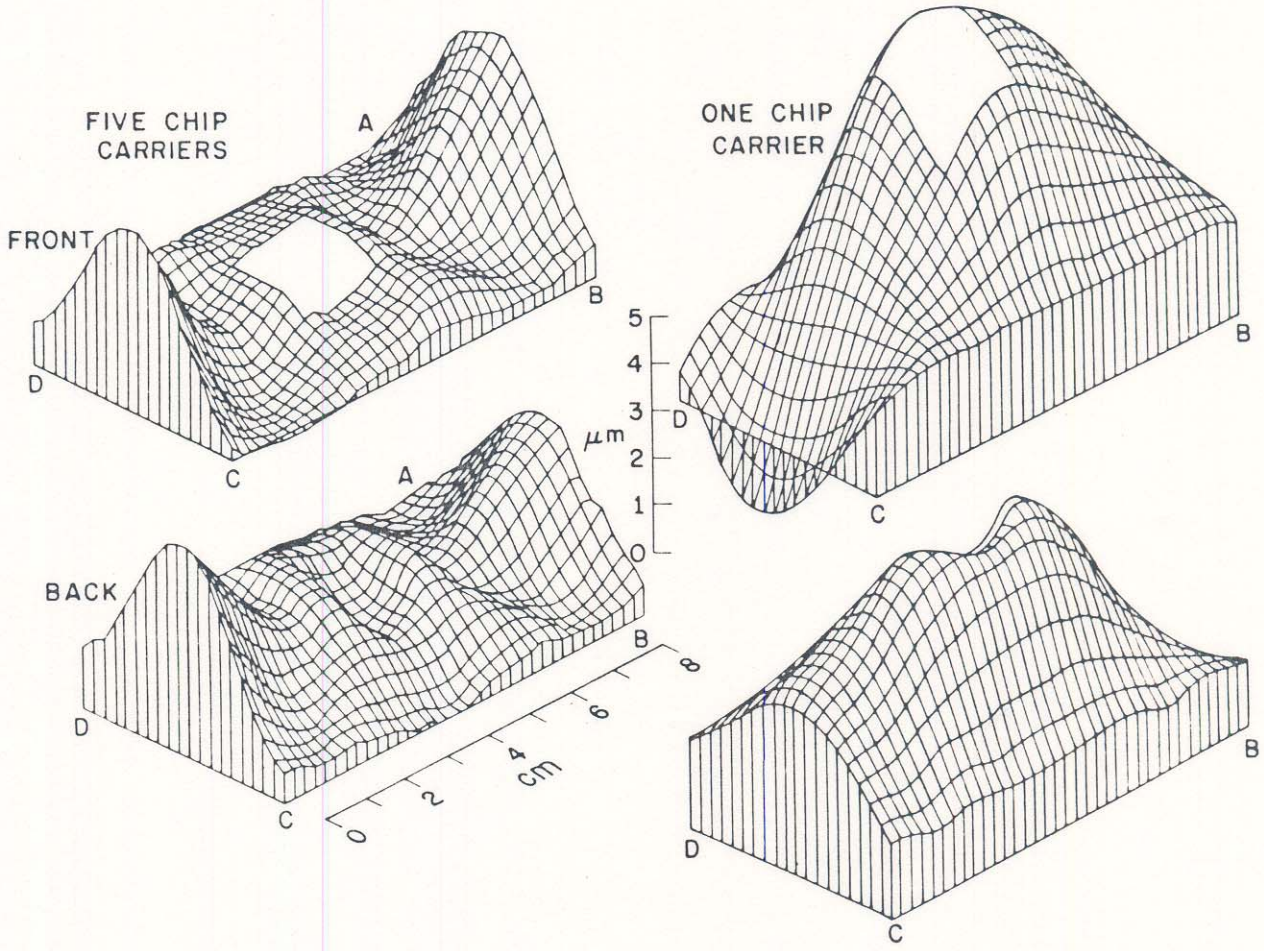

Figure 4. Isometric plots of the out-of-plane printed wiring board deformation distributions derived from the reconstructed holo-interferograms shown in Figure 2 for the prototype modules with no CCI sublayers in their printed wiring boards.

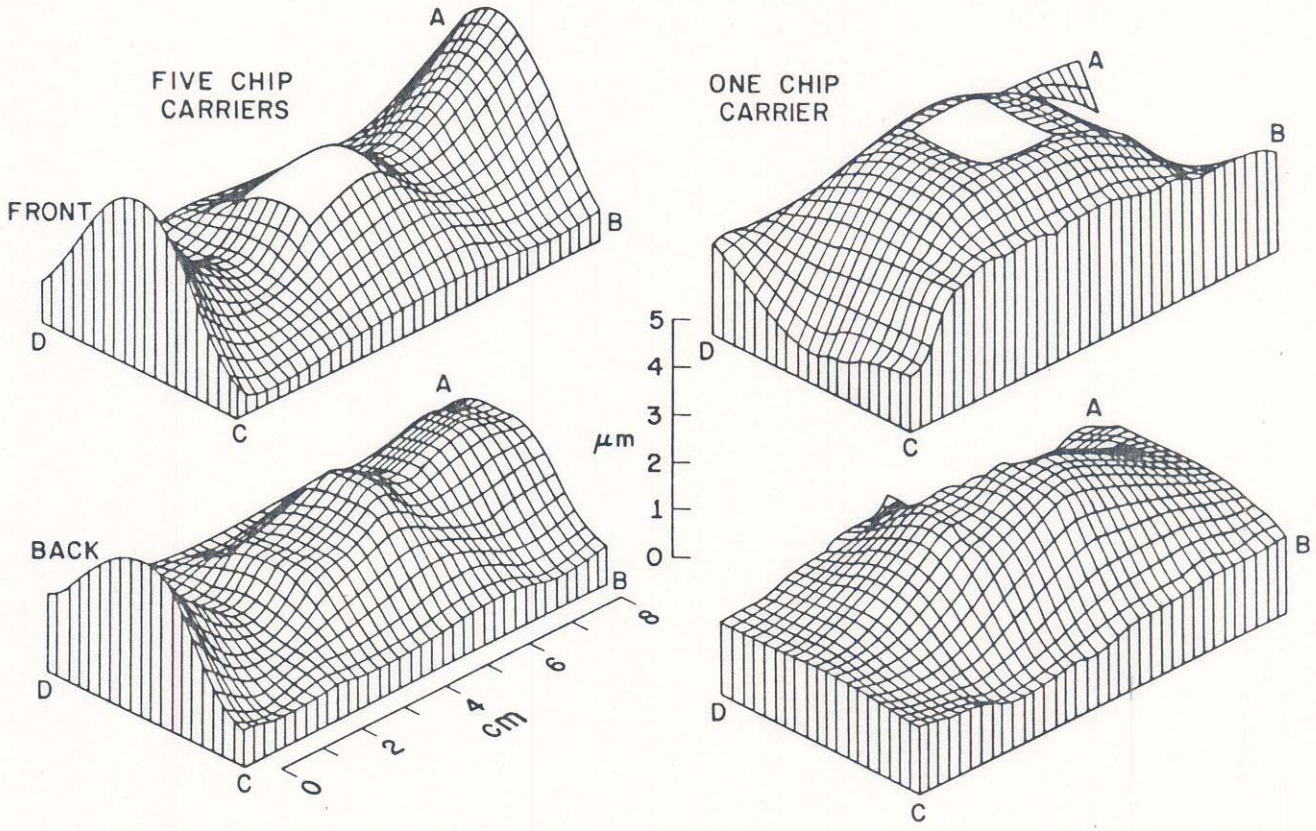

Figure 5. Isometric plots of the out-of-plane printed wiring board deformation distributions derived from the reconstructed holo-interferograms shown in Figure 3 for the prototype modules with CCI sublayers in their printed wiring boards.